

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A ~~predistorer~~ predistorter configured for use with an RF power amplifier, the predistorter comprising:
 - an input loop configured to be coupled to the input of an RF power amplifier, the input loop including a look-up table containing predistortion values, the input loop configured to apply the predistortion values to an input signal, in response to a monotonically increasing function of the input signal power, for forming a predistorted input signal; and
 - a peak control circuit coupled to the input loop, the peak control circuit configured to select a power supply voltage for the RF power amplifier in response to the power in the input signal; and
 - an output loop coupled to the output of the RF power amplifier, the output loop configured to measure an intermodulation distortion product of the RF power amplifier output resulting from the predistorted input signal, the output loop operable to update the predistortion values in the look-up table responsive to the measured intermodulation distortion product.
2. (Original) The predisorter of claim 1, wherein the monotonically increasing function of the input signal power includes at least one of the input power, the logarithm of the input power, and the square root of the input power.
3. (Canceled).

Page 2 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

4. (Currently Amended) The predistorter of claim 1 3, wherein the intermodulation distortion product is at least one of the third and the fifth intermodulation distortion products.
5. (Currently Amended) The predistorter of claim 1 3, wherein the output loop comprises:
- a coupler coupled to the output of the RF power amplifier;
 - a mixer coupled to the coupler;
 - a local oscillator coupled to the mixer and configured to output a frequency so that the mixer selects at least one of the third and the fifth intermodulation distortion products of the RF power amplifier;
 - an amplifier coupled to the mixer and configured to amplify at least one of the third and the fifth intermodulation distortion products;
 - a bandpass filter coupled to the amplifier and configured to frequency select at least one of the third and the fifth intermodulation distortion products;
 - an intermediate frequency to baseband converter circuit coupled to the bandpass filter and configured to produce a digital signal representative of the magnitude of at least one of the third and the fifth intermodulation distortion products; and
 - a processor coupled to the intermediate frequency to baseband converter circuit and the look-up table and configured to select an optimal set of predistortion values.
6. (Currently Amended) The predistorter of claim 1 3, wherein the output loop comprises a processor, the processor configured to select an optimal set of predistortion values using a gradient search.

Page 3 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

7. (Currently Amended) The predistorter of claim 1, wherein the output loop comprises a processor, the processor configured to apply a spline function to update predistortion values in the look-up table.
8. (Original) The predistorter of claim 7, wherein the application of the spline function involves analyzing amplitude to amplitude and amplitude to phase predistortion curves.
9. (Original) The predistorter of claim 7, wherein the spline function has knots and wherein the application of the spline function involves varying the magnitude of each knot, generating predistortion values, and measuring an intermodulation distortion product to determine whether the change in the magnitude of the knot improved the intermodulation distortion performance.
10. (Original) The predistorter of claim 7, wherein the look-up table has an index and the spline function includes knots that are placed along the look-up table index; and, wherein knot placement along the look-up table index is varied.
11. (Original) The predistorter of claim 1, wherein the input signal is of the type of at least one of $I+jQ$ and $A(t)\cos[\omega t+\theta(t)]$.
12. (Original) The predistorter of claim 1, wherein the input signal is of the type $I+jQ$, the predistortion values in the look-up table are in in-phase and quadrature-phase form, and the input loop comprises:
 - a magnitude detection circuit coupled to the look-up table and configured to produce a scalar value representative of the power of the input signal, the scalar value functioning as an index to the look-up table;
 - a complex multiplier coupled to the look-up table and configured to combine

Page 4 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

predistortion values in the look-up table with the input signal and output a predistortion signal;

first and second digital-to-analog converters coupled to the complex multiplier and configured to convert the predistortion signal from a digital signal to analog signals;

quadrature modulator coupled to the first and second digital-to-analog converters and configured to apply the analog signals to a carrier signal; and

an RF oscillator coupled to the quadrature modulator and configured to provide a carrier signal.

13. (Withdrawn) The predistorter of claim 1, wherein the input signal is of the type $I+jQ$, the predistortion values in the look-up table are in the form of magnitude and phase, and the input loop comprises:

a first converter circuit coupled to the look-up table and configured to convert the input signal into magnitude and phase form, the magnitude functioning as an index to the look-up table;

a multiplier circuit coupled to the first converter circuit and the look-up table, the multiplier circuit configured to combine a magnitude predistortion value in the look-up table with the magnitude of input signal;

an adder circuit coupled to the first converter circuit and the look-up table, the adder circuit configured to combine a phase predistortion value in the look-up table with the phase of input signal;

a second converter circuit coupled to the multiplier circuit and the adder circuit and configured to output a predistortion signal;

first and second digital-to-analog converters coupled to the second converter circuit and configured to convert the predistortion signal from a digital signal to analog signals;

Page 5 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

a quadrature modulator coupled to the first and second of digital-to-analog converters and configured to apply the analog signals to a carrier signal; and
an RF oscillator coupled to the quadrature modulator and configured to provide a carrier signal.

14. (Withdrawn) The predistorter of claim 1, wherein the input signal is of the type $A(t)\cos[\omega t + \theta(t)]$, the predistortion values in the look-up table are in the form of magnitude and phase, and the input loop comprises:

an envelope detection circuit coupled to the look-up table and configured to produce a scalar value representative of the power of the input signal;

an analog-to-digital converter circuit coupled to the detector circuit and the look-up table, the analog-to-digital converter circuit configured to convert the scalar value to a digital signal that functions as an index to the look-up table;

a complex attenuator coupled to the look-up table and configured to combine predistortion values in the look-up table with the input signal; and

a delay circuit coupled to the complex attenuator and configured to delay the application of the input signal to the complex attenuator.

15. (Withdrawn) The predistorter of claim 14, wherein the complex attenuator comprises:
a power attenuator; and
a phase shifter.

16. (Withdrawn) The predistorter of claim 14, wherein the complex attenuator comprises a vector modulator.

17. (Original) The predistorter of claim 1, wherein the peak control circuit comprises:
a threshold detector configured with at least one of a high power threshold

Page 6 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

and a low power threshold; and,

a power supply having a nominal voltage and a selectable voltage based on at least one of the high power threshold and the low power threshold.

18. (Currently Amended) An amplifier system comprising an RF power amplifier and a predistorter, the predistorter comprising:

an input loop configured to be coupled to the input of an RF power amplifier, the input loop including a look-up table containing predistortion values, the input loop configured to apply the predistortion values to an input signal, in response to a monotonically increasing function of the input signal power, for forming a predistorted input signal; and

a peak control circuit coupled to the input loop, the peak control circuit configured to select a power supply voltage for the RF power amplifier in response to the power in the input signal; and

an output loop coupled to the output of the RF power amplifier, the output loop configured to measure an intermodulation distortion product of the RF power amplifier output resulting from the predistorted input signal, the output loop operable to update the predistortion values in the look-up table responsive to the measured intermodulation distortion product.

19. (Original) The amplifier system of claim 18, wherein the monotonically increasing function of the input signal power includes at least one of the input power, the logarithm of the input power, and the square root of the input power.

20. (Canceled).

Page 7 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

21. (Currently Amended) The amplifier system of claim 18 20, wherein the intermodulation distortion product is at least one of the third and the fifth intermodulation distortion products.

22. (Currently Amended) The amplifier system of claim 18 20, wherein the output loop comprises:

a coupler coupled to the output of the RF power amplifier;

a mixer coupled to the coupler;

a local oscillator coupled to the mixer and configured to output a frequency so that the mixer selects at least one of the third and the fifth intermodulation distortion products of the RF power amplifier;

an amplifier coupled to the mixer and configured to amplify at least one of the third and the fifth intermodulation distortion products;

a bandpass filter coupled to the amplifier and configured to frequency select at least one of the third and the fifth intermodulation distortion products;

an intermediate frequency to baseband converter circuit coupled to the bandpass filter and configured to produce a digital signal representative of the magnitude of at least one of the third and the fifth intermodulation distortion products; and

a processor coupled to the intermediate frequency to baseband converter circuit and the look-up table and configured to select an optimal set of predistortion values.

23. (Currently Amended) The amplifier system of claim 18 20, wherein the output loop comprises a processor, the processor configured to select an optimal set of predistortion values using a gradient search.

Page 8 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 QA.wpd

24. (Currently Amended) The amplifier system of claim 18 20, wherein the output loop comprises a processor, the processor configured to apply a spline function to update predistortion values in the look-up table.
25. (Original) The amplifier system of claim 24, wherein the application of the spline function involves analyzing amplitude to amplitude and amplitude to phase predistortion curves.
26. (Original) The amplifier system of claim 24, wherein the spline function has knots and wherein the application of the spline function involves varying the magnitude of each knot, generating predistortion values, and measuring an intermodulation distortion product to determine whether the change in the magnitude of the knot improved the intermodulation distortion performance.
27. (Original) The amplifier system of claim 24, wherein the look-up table has an index and the spline function includes knots that are place along the look-up table index; and, wherein knot placement along the look-up table index is varied.
28. (Original) The amplifier system of claim 18, wherein the input signal is of the type of at least one of $I+jQ$ and $A(t)\cos[\omega t+\theta(t)]$.
29. (Original) The amplifier system of claim 18, wherein the input signal is of the type $I+jQ$, the predistortion values in the look-up table are in in-phase and quadrature-phase form, and the input loop comprises:
- a magnitude detection circuit coupled to the look-up table and configured to produce a scalar value representative of the power of the input signal, the scalar value functioning as an index to the look-up table;

Page 9 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO67US
K:\ANCO67US\Amendment and Response to 3-22-05 OA.wpd

a complex multiplier coupled to the look-up table and configured to combine predistortion values in the look-up table with the input signal and output a predistortion signal;

first and second digital-to-analog converters coupled to the complex multiplier and configured to convert the predistortion signal from a digital signal to analog signals;

a quadrature modulator coupled to the first and second digital-to-analog converters and configured to apply the analog signals to a carrier signal; and

an RF oscillator coupled to the quadrature modulator and configured to provide a carrier signal.

30. (Withdrawn) The amplifier system of claim 18, wherein the input signal is of the type $I+jQ$, the predistortion values in the look-up table are in the form of magnitude and phase, and the input loop comprises:

a first converter circuit coupled to the look-up table and configured to convert the input signal into magnitude and phase form, the magnitude functioning as an index to the look-up table;

a multiplier circuit coupled to the first converter circuit and the look-up table, the multiplier circuit configured to combine a magnitude predistortion value in the look-up table with the magnitude of input signal;

an adder circuit coupled to the first converter circuit and the look-up table, the adder circuit configured to combine a phase predistortion value in the look-up table with the phase of input signal;

a second converter circuit coupled the multiplier circuit and the adder circuit and configured to output a predistortion signal;

first and second digital-to-analog converters coupled to the second converter circuit and configured to convert the predistortion signal from a digital signal to

Page 10 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

analog signals;

a quadrature modulator coupled to the first and second digital-to-analog converters and configured to apply the analog signals to a carrier signal; and

an RF oscillator coupled to the quadrature modulator and configured to provide a carrier signal.

31. (Withdrawn) The amplifier system of claim 18, wherein the input signal is of the type $A(t)\cos[\omega t + \theta(t)]$, the predistortion values in the look-up table are in the form of magnitude and phase, and the input loop comprises:

an envelope detection circuit coupled to the look-up table and configured to produce a scalar value representative of the power of the input signal;

an analog-to-digital converter circuit coupled to the envelope detection circuit and the look-up table, the analog-to-digital converter circuit configured to convert the scalar value to a digital signal that functions as an index to the look-up table;

a complex attenuator coupled to the look-up table and configured to combine predistortion values in the look-up table with the input signal; and

a delay circuit coupled to the complex attenuator and configured to delay the application of the input signal to the complex attenuator.

32. (Withdrawn) The amplifier system of claim 31, wherein the complex attenuator comprises:

a power attenuator; and

a phase shifter.

33. (Withdrawn) The amplifier system of claim 31, wherein the complex attenuator comprises a vector modulator.

Page 11 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response to 3-22-05 OA.wpd

34. (Original) The amplifier system of claim 18, wherein the peak control circuit comprises:
- a threshold detector configured with at least one of a high power threshold and a low power threshold; and
 - a power supply having a nominal voltage and a selectable voltage based on at least one of the high power threshold and the low power threshold.
35. (Currently Amended) A method of predistorting an input signal applied to an RF power amplifier, the method comprising:
- producing a scalar value representative of the power of the input signal;
 - applying the scalar value to index a look-up table containing predistortion values;
 - combining the predistortion values with the input signal to improve the linearity of the RF power amplifier; and
 - applying the scalar to a threshold to select a power supply voltage for the RF power amplifier; and
 - measuring an intermodulation distortion product of the RF power amplifier to select optimal predistortion values based upon the measured intermodulation distortion product.
36. (Canceled).
37. (Currently Amended) The method of claim 35 36, wherein the intermodulation distortion product is at least one of the third and the fifth intermodulation distortion products.
38. (Original) The method of claim 35, wherein the optimal predistortion values are selected using a gradient search.

Page 12 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&B ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd

39. (Original) The method of claim 38, further comprising updating the predistortion values in the table.
40. (Original) The method of claim 38, wherein the predistortion values are updated by applying a spline function to the amplitude to amplitude and amplitude to phase characteristics of the RF power amplifier.
41. (Original) The method of claim 38, wherein the spline function has knots and wherein the application of the spline function involves varying the magnitude of each knot, generating predistortion values, and measuring an intermodulation distortion product to determine whether the change in the magnitude of the knot improved the intermodulation distortion performance.
42. (Original) The method of claim 38, wherein the spline function includes knots that are placed along the look-up table index; and, wherein knot placement along the look-up table index is varied.

Page 13 of 19
Serial No. 10/625,761
Amendment and Response dated June 22, 2005
Reply to Office Action of March 22, 2005
Andrew Docket #690 & #705
WH&E ANCO/67US
K:\ANCO\67US\Amendment and Response re 3-22-05 OA.wpd